

CLAIMS

1 *MJG1* > 1. A method of manufacturing a semiconductor component comprising:
2 providing a substrate with a surface;
3 providing a layer comprised of undoped gallium arsenide over the surface of the substrate;
4 forming a gate contact over a first portion of the layer; and
5 removing a second portion of the layer to expose a portion of the surface of the substrate.

6 2. The method of claim 1 wherein:

7 providing the layer further comprises providing the layer with a thickness of approximately
8 three to twelve nanometers.

9 3. The method of claim 1 wherein:

10 providing the layer further comprises providing the layer with a thickness of approximately
11 six to nine nanometers.

12 4. The method of claim 1 wherein:

13 forming the gate contact further comprises exposing the second portion of the layer.

14 5. The method of claim 1 wherein:

15 removing the second portion of the layer exposes a portion of the substrate.

16 6. The method of claim 1 further comprising:

1 implanting source and drain regions into the substrate after removing the second portion
2 of the layer.

3 7. The method of claim 1 further comprising:
4 implanting source and drain regions into the substrate before removing the second portion
5 of the layer.

6 8. The method of claim 1 further comprising:
7 forming a spacer adjacent to the gate contact after removing the second portion of the
8 layer.

9 9. The method of claim 1 further comprising:
10 forming a spacer adjacent to the gate contact before removing the second portion of the
11 layer.

12 10. The method of claim 9 further comprising:
13 keeping a third portion of the layer underneath the spacer after removing the second
14 portion of the layer.

15 11. The method of claim 1 wherein:
16 providing the substrate further comprises providing a delta-doped, heteroepitaxial
17 semiconductor structure for the substrate.

1 12. The method of claim 1 wherein:

2 providing the substrate further comprises:

3 providing a support layer;

4 providing a buffer layer overlying the support layer;

5 providing a doping layer overlying the buffer layer;

6 providing a spacer layer overlying the doping layer;

7 providing a channel layer overlying the spacer layer; and

8 providing a barrier layer overlying the channel layer.

9 13. The method of claim 1 wherein:

10 forming the gate contact further comprises:

11 forming the gate contact on the layer.

12 14. The method of claim 1 further comprising:

13 implanting source and drain regions into the substrate;

14 annealing the source and drain regions after removing the second portion of the layer; and

15 forming source and drain contacts over the source and drain regions after removing the

16 second portion of the layer.

17 15. The method of claim 1 wherein:

18 removing the second portion of the layer further comprises keeping the first portion of the

19 layer underneath the gate contact; and

removing the second portion of the layer further comprises keeping the first portion of the layer undoped.

16. A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-

5 doped, heteroepitaxial semiconductor substrate comprising:

6 a support layer comprised of semi-insulating gallium arsenide;

7 a buffer layer comprised of undoped gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping

layer;

an channel layer comprised of indium gallium arsenide and overlying the spacer

layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel

15 substrate;

16 providing an undoped gallium arsenide capping layer having a thickness of approximately
17 three to twelve nanometers and overlying the surface of the delta-doped, heteroepitaxial
18 semiconductor substrate;

19 forming a gate contact over the undoped gallium arsenide capping layer, the gate contact
20 covering a first portion of the undoped gallium arsenide capping layer and absent over a second
21 portion of the undoped gallium arsenide capping layer;

- 1 removing the second portion of the undoped gallium arsenide capping layer after forming
- 2 the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial
- 3 semiconductor substrate;
- 4 forming a spacer adjacent to the gate contact;
- 5 forming source and drain regions in the delta-doped, heteroepitaxial semiconductor
- 6 substrate; and
- 7 forming source and drain contacts over the source and drain regions after removing the
- 8 second portion of the undoped gallium arsenide capping layer.

17. The method of claim 16 wherein:

forming the source and drain regions further comprises implanting the source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate after removing the second portion of the undoped gallium arsenide capping layer; and

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide capping layer.

18. The method of claim 16 further comprising:

16 forming the source and drain regions further comprises implanting source and drain
17 regions into the delta-doped, heteroepitaxial semiconductor substrate before removing the second
18 portion of the undoped gallium arsenide capping layer;

19 forming the spacer further comprises forming a multi-layered spacer adjacent to the gate
20 contact before removing the second portion of the undoped gallium arsenide capping layer; and

1 keeping a third portion of the undoped gallium arsenide capping layer underneath the
2 multi-layered spacer after removing the second portion of the undoped gallium arsenide capping
3 layer.

Sub
19. The method of claim 16 wherein:

providing the undoped gallium arsenide capping layer further comprises providing the
6 undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

Sub
20. The method of claim 16 wherein:

providing the delta-doped, heteroepitaxial semiconductor substrate further comprises:

providing the buffer layer on the support layer and consisting essentially of gallium
10 arsenide;

providing the doping layer on the buffer layer and consisting essentially of silicon
12 and gallium arsenide;

providing the spacer layer on the doping layer and consisting essentially of gallium
14 arsenide;

providing the channel layer on the spacer layer and consisting essentially of indium
15 gallium arsenide; and

providing the barrier layer on the channel layer and consisting essentially of
17 aluminum gallium arsenide;

19 providing the undoped gallium arsenide capping layer further comprises:

20 providing the undoped gallium arsenide capping layer on the barrier layer;

21 forming the gate contact further comprises:

1 forming the gate contact on the first portion of the undoped gallium arsenide
2 capping layer; and

3 removing the second portion of the undoped gallium arsenide capping layer further
4 comprises:

5 removing the second portion of the undoped gallium arsenide capping layer to
6 expose a portion of the barrier layer.

7 21. The method of claim 20 further comprising:

8 annealing the source and drain regions after removing the second portion of the undoped
9 gallium arsenide capping layer,

10 wherein:

11 providing the undoped gallium arsenide capping layer further comprises providing
12 the undoped gallium arsenide capping layer with a thickness of approximately six to nine
13 nanometers.

14 22. A semiconductor component comprising:

15 a substrate with a surface;

16 a layer comprised of undoped gallium arsenide over a first portion of the surface of the
17 substrate; and

18 a gate contact over the layer,

19 wherein:

20 the layer is absent over a second portion of the substrate.

1 23. The semiconductor component of claim 22 wherein:

2 the layer has a thickness of approximately six to nine nanometers.

3 24. The semiconductor component of claim 22 wherein:

4 the layer has a thickness of approximately three to twelve nanometers; and

5 the substrate is a delta-doped, heteroepitaxial semiconductor substrate comprising:

6 a support layer comprised of semi-insulating gallium arsenide;

7 a buffer layer comprised of gallium arsenide overlying the support layer;

8 a doping layer delta-doped with silicon and overlying the buffer layer;

9 a spacer layer comprised of gallium arsenide and overlying the doping layer;

10 an channel layer comprised of indium gallium arsenide and overlying the spacer
11 layer; and

12 a barrier layer comprised of aluminum gallium arsenide and overlying the channel
13 layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor
14 substrate.

15 25. The semiconductor component of claim 24 further comprising:

16 source and drain regions in the substrate;

17 a multi-layered spacer adjacent to the gate contact; and

18 source and drain contacts overlying the source and drain regions.